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Date: June 23, 2006 / Carrie A. Patchin /
Carrie A. Patchin

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of:

Appellant(s): Michael P. Hills, *et al.*

Serial No: 10/083,098

Filing Date: February, 26, 2002

Examiner: Van H. Nguyen

Art Unit: 2194

Title: SMBUS NOTIFICATIONS

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Dear Sir:

Appellants submit this brief in connection with an appeal of the above-identified patent application. A credit card payment form is filed concurrently herewith in connection with all fees due regarding this appeal brief. In the event any additional fees may be due and/or are not covered by the credit card, the Commissioner is authorized to charge such fees to Deposit Account No. 50-1063 [MSFTP302US].

I. Real Party in Interest (37 C.F.R. §41.37(c)(1)(i))

The real party in interest in the present appeal is Microsoft Corporation, the assignee of the present application.

II. Related Appeals and Interferences (37 C.F.R. §41.37(c)(1)(ii))

Appellants, appellants' legal representative, and/or the assignee of the present application are not aware of any appeals or interferences which may be related to, will directly affect, or be directly affected by or have a bearing on the Board's decision in the pending appeal.

III. Status of Claims (37 C.F.R. §41.37(c)(1)(iii))

Claims 1-8 and 10-27 stand rejected by the Examiner. Claim 9 has been cancelled. The rejection of claims 1-8 and 10-27 is being appealed.

IV. Status of Amendments (37 C.F.R. §41.37(c)(1)(iv))

Amendments were made to claims 14, 24 and 27 after the Final Office Action dated December 30, 2005. The Examiner did not indicate whether the amendments would be entered or not.

V. Summary of Claimed Subject Matter (37 C.F.R. §41.37(c)(1)(v))

A. Independent Claim 1

Independent claim 1 recites a computer implemented system that facilitates AML access to an SMBus, comprising the following computer executable components: an AML event handler component; and, a driver component that identifies an SMBus event and dispatches the SMBus event to the AML event handler, where the AML event handler employs at least one of a three parameter buffer access read method to read data from an operation region associated with the SMBus and a three parameter buffer access write method to write data to an operation region associated with the SMBus. (*See e.g.*, page 6, line 28-page 7, line 1, page 7, lines 5-11)

B. Independent Claim 14

Independent claim 14 recites a computer readable medium holding computer executable components for a system that facilitates access to an SMBus, comprising: a computer executable

identifier that identifies an SMBus event notification at a driver; and a computer executable dispatcher in the driver that directly dispatches the SMBus event notification to a computer executable AML event handler.. (*See e.g.*, page 1, lines 29-31, page 9, lines 16-18)

C. Independent Claim 15

Independent claim 15 recites a computer implemented method for SMBus event handling, the method comprising the following computer executable acts: receiving an SMBus event notification at a driver; identifying the SMBus event notification; dispatching the SMBus event notification to an AML event handler; and handling the SMBus event notification in AML code. (*See e.g.*, page 1, lines 29-31)

D. Claim 19

Claim 19 recites he method of claim 18, where the operation region is accessed by a three parameter read, where a first parameter holds an initial data, a second parameter holds a reference to the operation region to be accessed and a third parameter holds data read from the operation region.. (*See e.g.*, page 7, line 27-page 8, line 5)

E. Claim 20

Claim 20 recites the method of claim 18, where the operation region is accessed by a three parameter read, where a first parameter holds an initial data, a second parameter holds a reference to the operation region to be accessed and a third parameter holds a reference to data read from the operation region. (*See e.g.*, page 7, line 27-page 8, line 6)

F. Claim 22

Claim 22 recites the method of claim 21, where the operation region is written by a three parameter write, where a first parameter holds a data to be written to the operation region, a second parameter holds a reference to the operation region and a third parameter holds a returned status call. (*See e.g.*, page 8, lines 10-18)

G. Claim 23

Claim 23 recites The method of claim 21, where the operation region is written by a three parameter write, where a first parameter holds a reference to a data to be written to the operation region, a second parameter holds a reference to the operation region and a third parameter holds a returned status call. (*See e.g.*, page 8, lines 10-18).

H. Independent Claim 25

Independent claim 25 recites a computer executable system for SMBus event handling, comprising: computer implemented means for receiving an SMBus notification via a _Qxx control method; (*See e.g.*, page 9, lines 16-17, page 11, line 9) computer implemented means for locating an AML code event handler associated with the SMBus notification; and (*See e.g.*, page page 11, lines 20-22) computer implemented means for the _Qxx control method to dispatch the SMB notification to the AML code event handler associated with the SMBus notification. (*See e.g.*, page 9, lines 16-18, page 11, lines 24-25).

The means for limitations described above are identified as limitations subject to the provisions of 35 U.S.C. §112 ¶6. The structures corresponding to these limitations are identified with reference to the specification and drawings in the above-noted parentheticals.

G. Independent Claim 27

Independent claim 27 recites a data structure employed by computer implemented processes executing on a computer readable medium that facilitates dispatching an SMBus event to an AML code event handler, the data structure comprising: at least one indexed AML code entry point; and at least one AML event handler entry point associated with the at least one indexed AML code entry point. (*See e.g.*, page 12, lines 9-14)

VI. Grounds of Rejection to be Reviewed (37 C.F.R. §41.37(c)(1)(vi))

A. Whether claims 1-8 and 10-27 are unpatentable under 35 U.S.C. §102(b) over Lewis (US Patent 6,167,511).

VII. Argument (37 C.F.R. §41.37(c)(1)(vii))

A. Rejection of Claims 1-8 and 10-13 Under 35 U.S.C. §102(b)

Claims 1-8 and 10- 13 stand rejected under 35 U.S.C. §102(b) as being anticipated by Lewis (US 6,167,511). It is respectfully submitted that this rejection should be reversed for at least the following reasons. Lewis does not teach or suggest each and every limitation of appellants' claimed invention.

> A single prior art reference anticipates a patent claim only if it expressly or inherently describes ***each and every*** limitation set forth in the patent claim. *Trintec Industries, Inc. v. Top-U.S.A. Corp.,* 295 F.3d 1292, 63 USPQ2d 1597 (Fed. Cir. 2002); *See Verdegaal Bros. v. Union Oil Co. of California,* 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the … claim. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

The subject application relates to SMBus (System Management Bus) event notification handling and relates more particularly to handling SMBus event notification in ASL (ACPI Source Language) code, which is compiled into AML (ACPI Machine Language) code eliminating the need for the ASL code to manipulate lower level hardware, such as an embedded controller. Furthermore, appellants' claimed invention teaches three parameter buffer access read and write methods capable of transferring variable sized blocks that allow for more efficient and simplified data transfers. In particular, independent claim 1 recites ***an AML event handler component; and, a driver component that identifies an SMBus event and dispatches the SMBus event to the AML event handler, where the AML event handler employs at least one of a three parameter buffer access read method to read data from an operation region associated with the SMBus and a three parameter buffer access write method to write data to an operation region associated with the SMBus***.

Contrary to assertions in the Office Action, Lewis does not teach or suggest the aforementioned novel aspects of appellants' invention as recited in the subject claims. Lewis teaches a system for modifying AML code in run-time based upon changes that are made in the BIOS setup. In connection with the invention recited in these claims, a driver component receives an SMBus event notification and dispatches the event to the AML event handler for

appropriate event processing. This system improves performance by allowing the driver, running in native machine code, to access the SMBus instead of an interpreted AML code utilizing an ACPI specified embedded controller. Lewis does not teach or suggest such novel features of appellants' claimed invention. The section of the reference beginning at column7, line 36 cited in the Office Action relates to a general description of fixed feature event processing and *discloses that events are processed by a single component, which is the ACPI driver that also acts as the event handler*. Lewis is silent regarding the ACPI driver having access to the SMBus to identify event notifications and passing event notifications to a separate AML event handler component. Moreover, Lewis also fails to disclose a three parameter buffer access read that is employed by the AML event handler. The section of the cited art referenced by the Examiner beginning at column 8, line 23 discloses a method for relocating register blocks. The method involves reading a table, one entry at a time, to locate a particular value. When an appropriate entry is located, the register block routine is called with two parameters, a length field and an index field. This is not a three parameter buffer access read. Lewis is silent regarding a three parameter buffer access *read* and particularly one that is employed by an AML event handler. In addition, the prior art reference also fails to disclose a three parameter buffer access *write* that is employed by the AML event handler. The Examiner cites a section of the reference that discloses a method for integrating Motherboard Configurable Devices (MCD) into ACPI - this section of the reference (let alone any section of the prior art) does not discuss AML event handling and is silent regarding three parameter buffer access writes.

In view of at least the above, it is respectfully submitted that Lewis does not teach or suggest appellants' invention as recited in independent claim 1 (and claims 2-8 and 10-13 which respectively depend there from). Accordingly, reversal of this rejection is respectfully requested.

B. Rejection of Claims 14-24 Under 35 U.S.C. §102(b)

Claims 14-24 stand rejected under 35 U.S.C. §102(b) as being anticipated by Lewis. It is respectfully submitted that this rejection should be reversed for at least the following reasons. Lewis does not teach or suggest each and every limitation of appellants' claimed invention.

Independent claim 14 (and similarly independent claim 15) recites ***a computer executable identifier that identifies an SMBus event notification at a driver and a computer executable dispatcher in the driver that directly dispatches the SMBus event notification to a***

computer executable AML event handler. As discussed above with respect to independent claim 1, Lewis fails to teach this novel feature similarly recited in independent claims 14 and 15. Moreover, dependent claims 19, 20, 22 and 23 recite specific parameters associated with the three parameter operation region read and write accesses. As noted *supra* with respect to independent claim 1, Lewis fails to disclose three parameter read and write accesses. Furthermore, Lewis is silent regarding the specific three parameters recited in the limitations of each of claims 19, 20, 22 and 23.

Accordingly, it is respectfully submitted that Lewis does not teach or suggest appellants' invention as recited in independent claims 14 and 15 (and claims 16-24 which respectively depend there from). Therefore, reversal of this rejection is respectfully requested.

C. Rejection of Claims 25 and 26 Under 35 U.S.C. §102(b)

Claims 25 and 26 stand rejected under 35 U.S.C. §102(b) as being anticipated by Lewis. It is respectfully submitted that this rejection should be reversed for at least the following reasons. Lewis does not teach or suggest each and every limitation of appellants' claimed invention.

Independent claim 25 recites *means for receiving an SMBus notification* ***via a _Qxx control method****; means for locating an AML code event handler associated with the SMBus notification; and means for* ***the _Qxx control method to dispatch the SMB notification to the AML code event handler*** *associated with the SMBus notification*. Appellants' claimed invention discloses a system where an SMBus event notification is received by a control method and passed to the AML event handler for processing, in lieu of being received by an embedded controller. Although Lewis summarizes parts of the ACPI specification in the "Background of the Invention" section of the patent which discloses higher level control methods, Lewis fails to teach or suggest a control method that receives a SMBus event notification or a control method that passes a SMBus notification to an AML event handler. This section merely describes in general terms how the ACPI specification allows the operating system to have greater control over resources without any specific disclosure of the control methods recited in the subject claim.

Accordingly, this rejection should be reversed.

D. Rejection of Claim 27 Under 35 U.S.C. §102(b)

Claim 27 stands rejected under 35 U.S.C. §102(b) as being anticipated by Lewis. It is respectfully submitted that this rejection should be reversed for at least the following reasons. Lewis does not teach or suggest each and every limitation of appellants' claimed invention.

Independent claim 27 recites *a data structure employed by computer implemented processes executing on a computer readable medium that facilitates dispatching an SMBus event to an AML code event handler,* ***the data structure comprising: at least one indexed AML code entry point; and at least one AML event handler entry point associated with the at least one indexed AML code entry point***. Lewis is silent regarding a data structure that contains at least one indexed AML code entry point; and at least one AML event handler entry point associated with the at least one indexed AML code entry point. Therefore, reversal of this rejection is respectfully requested.

E. Conclusion

For at least the above reasons, the claims currently under consideration are believed to be patentable over the cited references. Accordingly, it is respectfully requested that the rejections of claims 1-8 and 10-27 be reversed.

If any additional fees are due in connection with this document, the Commissioner is authorized to charge those fees to Deposit Account No. 50-1063 [MSFTP302US].

Respectfully submitted,
AMIN, TUROCY & CALVIN, LLP

/Himanshu S. Amin/
Himanshu S. Amin
Reg. No. 40,894

AMIN, TUROCY & CALVIN, LLP
24th Floor, National City Center
1900 East 9th Street
Telephone: (216) 696-8730
Facsimile: (216) 696-8731

VIII. Claims Appendix (37 C.F.R. §41.37(c)(1)(viii))

1. A computer implemented system that facilitates AML access to an SMBus, comprising the following computer executable components:

an AML event handler component; and,

a driver component that identifies an SMBus event and dispatches the SMBus event to the AML event handler, where the AML event handler employs at least one of a three parameter buffer access read method to read data from an operation region associated with the SMBus and a three parameter buffer access write method to write data to an operation region associated with the SMBus.

2. The system of claim 1, where the driver receives a status and a data associated with the SMBus event from the SMBus.

3. The system of claim 1, where the driver employs a _Qxx control method to dispatch the SMBus event to the AML event handler.

4. The system of claim 1, where at least one AML event handler entry point is accessed by the _Qxx control method.

5. The system of claim 4, where a first parameter of the three parameter buffer access read method provides an initial data to a computer component providing access to the operation region associated with the SMBus.

6. The system of claim 5, where a second parameter of the three parameter buffer access read method is a reference to the operation region associated with the SMBus from which the data will be read.

7. The system of claim 6, where a third parameter of the three parameter buffer access read method holds data read from the operation region identified by the second parameter.

8. The system of claim 6, where a third parameter of the three parameter buffer access read method is a reference to a location to store the data read from the operation region identified by the second parameter.

9. (Cancelled)

10. The system of claim 1, where a first parameter of the three parameter buffer access write method is the data to be written to the operation region associated with the SMBus.

11. The system of claim 1, where a first parameter of the three parameter buffer access write method is a reference to the data to be written to the operation region associated with the SMBus.

12. The system of claim 1, where a second parameter of the three parameter buffer access write method is a reference to the operation region associated with the SMBus to which the data will be written.

13. The system of claim 1, where a third parameter of the three parameter buffer access write method is a status code returned by a computer component providing access to the operation region associated with the SMBus.

14. A computer readable medium holding computer executable components for a system that facilitates access to an SMBus, comprising:

a computer executable identifier that identifies an SMBus event notification at a driver; and

a computer executable dispatcher in the driver that directly dispatches the SMBus event notification to a computer executable AML event handler.

15. A computer implemented method for SMBus event handling, the method comprising the following computer executable acts:

receiving an SMBus event notification at a driver;

identifying the SMBus event notification;

dispatching the SMBus event notification to an AML event handler; and

handling the SMBus event notification in AML code.

16. The method of claim 15, where the SMBus event notification is identified by examining at least one of a data and a status associated with the SMBus event notification.

17. The method of claim 15, where dispatching the SMBus event notification comprises indexing to a _Qxx control method via a registered AML event handler.

18. The method of claim 15, where handling the SMBus event notification in AML code comprises reading an operation region associated with the SMBus that generated the SMBus notification.

19. The method of claim 18, where the operation region is accessed by a three parameter read, where a first parameter holds an initial data, a second parameter holds a reference to the operation region to be accessed and a third parameter holds data read from the operation region.

20. The method of claim 18, where the operation region is accessed by a three parameter read, where a first parameter holds an initial data, a second parameter holds a reference to the operation region to be accessed and a third parameter holds a reference to data read from the operation region.

21. The method of claim 15, where handling the SMBus event notification in AML code comprises writing an operation region associated with the SMBus that generated the SMBus notification.

22. The method of claim 21, where the operation region is written by a three parameter write, where a first parameter holds a data to be written to the operation region, a second parameter holds a reference to the operation region and a third parameter holds a returned status call.

23. The method of claim 21, where the operation region is written by a three parameter write, where a first parameter holds a reference to a data to be written to the operation region, a second parameter holds a reference to the operation region and a third parameter holds a returned status call.

24. A computer readable medium storing computer instructions operable to perform the method of claim 15.

25. A computer executable system for SMBus event handling, comprising:

computer implemented means for receiving an SMBus notification via a _Qxx control method;

computer implemented means for locating an AML code event handler associated with the SMBus notification; and

computer implemented means for the _Qxx control method to dispatch the SMB notification to the AML code event handler associated with the SMBus notification.

26. The system of claim 25, comprising means for the AML code event handler to access a data object employed to communicate with an SMBus.

27. A data structure employed by computer implemented processes executing on a computer readable medium that facilitates dispatching an SMBus event to an AML code event handler, the data structure comprising:

at least one indexed AML code entry point; and

at least one AML event handler entry point associated with the at least one indexed AML code entry point.

IX. Evidence Appendix (37 C.F.R. §41.37(c)(1)(ix))

None.

X. Related Proceedings Appendix (37 C.F.R. §41.37(c)(1)(x))

None.